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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,755	10/22/2003	Barton E. Bennett	OTC0001	5377

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BAKER & DANIELS LLP
205 W. JEFFERSON BOULEVARD
SUITE 250
SOUTH BEND, IN 46601

EXAMINER	
NGUYEN, HOA CAO	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,755	BENNETT, BARTON E.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1 pg*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *2 pgs*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election of claims 1-14 in the reply filed on 2/21/06 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Applicant has amended claims 15 and requested that group II, claims 15-20, be reconsidered for examination together with group I, claims 1-14. The amended group II, claims 15-20, has been fully considered but they are not persuasive for examination together with group I because of the following reasons:

The application contains claims directed to the following patentably distinct species:

Specie I: Figures 2 and 3 disclose a structure of multilayer circuit board with embedded electronic components and the structure further contains a heat dissipation device (heat sink and heat sink lead).

Specie II: At least figures 8-16 disclose a structure of multilayer circuit board with embedded electronic components and the structure further contain a support structure (a truss element) and the electronic components are also formed on the support structure and the circuit board is cooled by air (a gap between layers for air circulation - materials being porous to allow air for cooling).

The species are independent or distinct because each draws to a different structure for the embedding electronic components.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, claim 1 is generic.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Thus, the requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Mowatt et al. (US 5432677).

Regarding claim 1, as shown in figure 6, Mowatt et al. disclose a composite sandwich structure with embedded electronics comprising:

(a) First and second multilayer composite facesheet laminates 124/150 (column 8, lines 37 and 60-65 and column 9, lines 2-2) made of structural fiber reinforced material (composite material, column 2, lines 46-48);

(b) first and second multilayer circuit laminates 126/138/16/22 (column 8, lines 49-51and column 5, lines 2-7) made of low dielectric fiber reinforced material (polymere for example, column 2, lines 60-62) with electrically conducting printed circuits 12/18/20/128/130/132/134/136/140/142/146/148 (conductive layers - column 5, lines 19-25 and interconnect structure - column 8, lines 34-54 and column 7, lines 50-64) embedded between low dielectric plies;

(c) a core structure 10 (a laminate layer, see abstract);

(d) electronic components 56 (a chip, see abstract) located in a central region where the core structure is located and having electrical conducting pins 36/38/40 (conductive vias, column 6, line 14) in contact with and secured to the printed circuits within either of the multilayer circuit laminates.

It is noticed that the conductive vias including interconnecting vias are considering as conductive pins (metal materials). Furthermore, as shown in figure 7, Mowatt et al. also disclose leads 162/164 soldered to the plated through holes 38 and 40 (column 9, lines 20-21).

Regarding claims 2-5, Mowatt et al. disclose the reinforce material includes one of ceramic, glass, composite material, polymere material, polymide, teflon or other materials commonly in used in PWB fabrication. It is also noticed that woven or non-woven dielectric material (non-woven glass fiber for example) is also conventionally known in the art.

Regarding claim 6, as shown in figure 6, Mowatt et al. disclose the first and second multilayer circuit laminates that are located on opposite sides of the core structure, and the multilayer circuit laminates in the core structure are

sandwiched between the first and second multilayer composite facesheet laminates.

Regarding claims 7-9, as shown in figure 6, Mowatt et al. disclose the first multilayer composite facesheet laminate which is inherently bonded to the first multilayer circuit laminate, and the second multilayer composite facesheet laminate is inherently bonded to the second multilayer circuit laminate (see adhesive layers in column 3, lines 18-35). It is noticed that adhesive is a resin (see column 7, line 26) and the resin must be cured after bonding.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mowatt et al. in view of common knowledge and in view of Sugaya et al (US 6538210).

Regarding claims 10-11, Mowatt et al. disclose every limitation as shown in claim 1 above but failed to disclose the redundant circuitry and components and a signal control device to sense if the equivalent components of circuitry have malfunctioned or failed and a switch to electronically reconfigure the circuitry to isolate the equivalent components or circuitry that have malfunctioned or failed and activate the redundant circuitry and components.

It is old and known in the art to have a redundant circuitry to function in case of failure of other components in order to continue the design functionality of the device. Therefore, it is obvious to have the above redundant circuitry.

Furthermore, the limitation about the redundant circuitry and components and a signal control device to sense if the equivalent components of circuitry have malfunctioned or failed and a switch to electronically reconfigure the circuitry to isolate the equivalent components or circuitry that have malfunctioned or failed and activate the redundant circuitry and components **is interpreted to only require the ability to so perform. In the case of product claim, only the structure of the claim distinguishes over the prior art.**

Regarding claim 12, Mowatt et al. disclose every limitation as shown in claim 1 above but failed to disclose at least one heat sink lead thermally connected to a heat generating electronic component within the composite sandwich structure and thermally connected to a heat sink outside the composite sandwich structure. However, Mowatt et al. do disclose a heat sink 156 formed outside the structure.

Sugaya et al., as shown in figure 7, disclose a semiconductor device 709 embedded within an insulating substrate 701 and a plurality of thermal vias 708 penetrated through the substrate and coupled to the device to draw heat away from the device and the heat is released through releasing heat layers 702aa and 702bb formed on a surface of the substrate (see column 21, lines 25-39). Sugaya et al. also disclose how the thermal is formed (see column 7, lines 35-62), which is mainly contained metal particles mixed with conductive resin (also see column 23, lines 34-36).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings from Sugaya et al. to formed at least a heat sink lead, which is a thermal via, penetrating through the second multilayer composite facesheet laminates 124 and the second multilayer circuit laminates 16/22 to thermally couple the heat sink 156 and the electronic component 56 in order to be more efficiently drawing heat away from the component 56 to the heat sink 156. It is also noticed that, as shown in figure 7 of Mowatt et al., the heat generated by the device 56 must travel through a multilayer substrate before reaching the heat sink; therefore the forming of heat sink lead, as taught by Sugaya et al., is far more efficient.

Regarding claims 13-14, Mowatt et al. in view of Sugaya et al. disclose every limitation as discussed in claim 12 above.

Citation of Relevant Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Platt (US 6292366) discloses a printed circuit board with embedded integrated circuit.

Sawamura (US 5997998) discloses a resistance element.

Singhdeo (US 4739443) discloses a thermally conductive module.

Nakatani et al. (US 20020117743) disclose a component built-in module and method for producing the same.

Sugaya et al. (US 6784530) disclose a circuit component built-in module with embedded semiconductor chip and method of manufacturing.

Akram et al. (US 6222265) disclose a method of constructing stacked packages.

Nabemoto et al. (US 6625880) disclose a method for producing printed wiring board.

Akram et al. (US 6404044) disclose a semiconductor package with stacked substrates and multiple semiconductor dice.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
3/28/06

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800